CLAIMS

What is claimed is:

1. A method of manufacturing, comprising:

forming a gate structure on a semiconductor portion of a substrate, the semiconductor portion having a first conductivity type;

forming first and second spacer structures on opposite sides of the gate structure;

forming a first impurity region of a second conductivity type proximate the first spacer structure while masking the semiconductor portion lateral to the second spacer structure, the first impurity region and the semiconductor portion defining a junction;

reducing a width of the second spacer structure while masking the second spacer structure and the first impurity region; and

forming a second impurity region of the first conductivity type in the semiconductor portion proximate the second spacer structure.

2. The method of claim 1, wherein the forming of the first and second spacer structures comprises forming first and second spacers on the opposite sides of the gate structure, and forming third and fourth spacers on opposite sides of the first and second spacers.

3. The method of claim 2, wherein the reducing a width of the second spacer structure comprises removing the fourth spacer.

4. The method of claim 2, comprising forming fifth and sixth spacers respectively between the first and third spacers and the second and fourth spacers.

5. The method claim 4, wherein the reducing a width of the second spacer structure comprises etching the fourth spacer selectively to the sixth spacer.

6. The method of claim 1, wherein forming the first impurity region comprises implanting an impurity, the second conductivity type being p-type, the junction being a pn junction.

7. The method of claim 1, wherein the reducing of the width of the second spacer structure comprises etching the second spacer structure.

8. The method of claim 1, wherein the forming of the second impurity region comprise implanting an impurity.

9. The method claim 1, comprising forming a circuit device on the substrate.

10. The method of claim 9, wherein the forming of the circuit device comprises forming a transistor.

11. A method of manufacturing a diode, comprising:

forming a gate structure on a semiconductor portion of a substrate, the semiconductor portion having a first conductivity type;

forming first and second spacer structures on opposite sides of the gate structure;

forming a first impurity region of a second conductivity type proximate the first spacer structure while masking the semiconductor portion lateral to the second spacer structure, the first impurity region and the semiconductor portion defining a pn junction;

reducing a width of the second spacer structure while masking the second spacer structure and the first impurity region; and

forming a second impurity region of the first conductivity type in the semiconductor portion proximate the second spacer structure but in spaced-apart relation to the pn junction.

12. The method of claim 11, wherein the forming of the first and second structures comprises forming first and second spacers on the opposite sides of the gate structure, and forming third and fourth spacers on opposite sides of the first and second spacers.

13. The method of claim 12, wherein the reducing a width of the second spacer structure comprises removing the fourth spacer.

14. The method of claim 12, comprising forming fifth and sixth spacers respectively between the first and third spacers and the second and fourth spacers.

15. The method claim 14, wherein the reducing a width of the second spacer structure comprises etching the fourth spacer selectively to the sixth spacer.

16. The method of claim 11, wherein forming of the first impurity region comprises implanting an impurity, the second conductivity type being p-type, the junction being a pn junction.

17. The method of claim 11, wherein the reducing of the width of the second spacer structure comprises etching the second spacer structure.

18. The method of claim 11, wherein the forming of the second impurity region comprises implanting an impurity.

19. The method claim 11, comprising forming a circuit device on the substrate.

20. The method of claim 19, wherein the forming of the circuit device comprises forming a transistor.

21. The method of claim 11, comprising forming an ohmic contact to the second impurity region.

22. The method of claim 21, comprising electrically connecting the gate and the ohmic contact.

23. A circuit device, comprising:
a substrate having a semiconductor portion of a first conductivity type;
a gate structure on the semiconductor portion;
first and second spacer structures on opposite sides of the gate structure, the second spacer structure being narrower than the first spacer structure;
a first impurity region of a second conductivity type in the semiconductor portion proximate the first spacer structure, the first impurity region and the semiconductor portion defining a pn junction;
a second impurity region of the first conductivity type in the semiconductor portion proximate the second spacer structure but in spaced-apart relation to the pn junction.

24. The circuit device of claim 23, wherein the substrate comprises a semiconductor-on-insulator substrate.

25. The circuit device of claim 23, wherein the semiconductor portion comprises silicon.

26. The circuit device of claim 23, wherein the first spacer structures comprises first, second, third and fourth spacers and the second spacer structure comprises fifth and sixth spacers.

27. The circuit device of claim 23, wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type.

28. The circuit device of claim 23, wherein the second impurity region has a lateral boundary positioned closer to the gate structure than the pn junction.

29. The circuit device of claim 23, comprising a conductor coupled to the gate structure and the second impurity region.

30. The circuit device of claim 29, wherein the gate structure is grounded.

31. The circuit device of claim 23, comprising a transistor on the substrate.

32. A diode, comprising:
a substrate having a semiconductor portion with an n-type doping;
a gate structure on the semiconductor portion;
first and second spacer structures on opposite sides of the gate structure, the second spacer structure being narrower than the first spacer structure;
a p-type impurity region in the semiconductor portion proximate the first spacer structure, the p-type impurity region and the semiconductor portion defining a pn junction;
an n-type impurity region in the semiconductor portion proximate the second spacer structure but in spaced-apart relation to the pn junction.

33. The diode of claim 32, wherein the substrate comprises a semiconductor-on-insulator substrate.

34. The diode of claim 32, wherein the semiconductor portion comprises silicon.

35. The diode of claim 32, wherein the first spacer structures comprises first, second, third and fourth spacers and the second spacer structure comprises fifth and sixth spacers.

36. The diode of claim 32, wherein the second impurity region has a lateral boundary positioned closer to the gate structure than the pn junction.

37. The diode of claim 32, comprising a conductor coupled to the gate structure and the n-type impurity region.

38. The diode of claim 37, wherein the gate structure is grounded.

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39. The diode of claim 32, comprising a transistor on the substrate.